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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/765,907	01/19/2001	Stephen M. Trimberger	X-714 US	9367

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EXAMINER	
COLIN, CARL G	

ART UNIT	PAPER NUMBER
2136	

MAIL DATE	DELIVERY MODE
08/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/765,907	TRIMBERGER, STEPHEN M.	
	Examiner	Art Unit	
	Carl Colin	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,12,13,15,21 and 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7, 12-13, 15, 21, and 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 6/8/2007, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Response to Arguments

2. Applicant's arguments, in the appeal brief, filed on 6/8/2007, with respect to the rejection of claims 1 and 44 have been fully considered, but they are moot in view of a new ground of rejection. In response to Applicant's arguments regarding claims 7 and 21 that the prior art does

not disclose the oscillator comprises configurable logic blocks. It is noted that these features are well-known in the art as set forth below. The following claims 1-4, 7, 12-13, 15, 21, and 44 are pending for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 12-13, 15, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patent 5,963,043 to **Nassif** in view of US Patent 5,970,142 to **Erickson** in view of US Patent 6,233,339 to **Kawano et al**.

As per claim 1, Nassif substantially discloses a method comprising: counting a first number of oscillations of a first oscillator on the integrated circuit (see column 4, lines 56-67) and the number of oscillations is counted over a fixed time interval (see column 4, lines 2-8) that meets the recitation of *counting a first number of oscillations of a first oscillator during a*

predetermined time interval and **Nassif** further discloses counting a second number of oscillations of a second oscillator on the integrated circuit (see column 4, lines 56-67) and the number of oscillations is counted over a fixed time interval (see column 4, lines 2-8) that meets the recitation of *counting a second number of oscillations of a second oscillator during a predetermined time interval;* **Nassif** discloses *generating a ratio between the first number and the second number of oscillations that represents an inherent manufacturing characteristic unique* (see column 4, lines 56-67). **Nassif** does not explicitly disclose the circuit is programmable (i.e. an FPGA). Use of programmable integrated circuit is notoriously well-known in the art of cryptography. **Erickson** in an analogous art teaches a programmable integrated circuit as an FPGA and method for securing data used to configure a PLD or FPGA (see column 1, lines 5-15 and line 59 through column 2, line 49). **Erickson** further discloses generating a key that meets the recitation of *fingerprint that represents an inherent manufacturing characteristic unique to the FPGA and transmitting encrypted configuration data from the storage device to the FPGA*, for example (see column 3, lines 34-36); and a decryption circuit coupled to received encrypted configuration data, the decryption circuit configured to *decrypt the encrypted configuration data in the FPGA using the fingerprint as a decryption key to extract the configuration data*, for example (see column 3, lines 34-42). See also column 2, lines 23-37. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of characterizing the circuit disclosed by **Nassif** into a programmable circuit so as to determine the performance of the circuit and to determine whether or not they exceed a certain design criteria as suggested by **Nassif** (see column 1, lines 15-30) and one of ordinary skill in the art would have recognized the benefits of

using as FPGA as taught by **Erickson** for protecting the circuit designs from illegal copying and use (see column 1, lines 26-39).

Nassif discloses generating a ratio from dividing the number of two oscillations from two oscillators and further discloses that the ratio of the oscillation periods is proportional to the ratio of the capacitance but does not explicitly disclose using the ratio of the oscillators or capacitance as a key or fingerprint for cryptographic operation such as decryption of encrypted data. **Kawano et al** in an analogous art teaches using the ratio of the capacitance for forming a specific code for the purpose of encryption/decryption (see column 19, lines 30-50 and column 26, lines 30-41). Therefore, since the ratio of the oscillation periods is proportional to the ratio of the capacitance, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the features as taught by **Kawano et al** of using the ratio of the capacitance as a fingerprint or key for the purpose of protecting secret data against intrusion (see column 1, lines 5-12) to modify **Nassif** and use the ratio of the oscillations as a fingerprint or key. As disclosed in **Kawano et al** the motivation for the combination would be to protect secret data against intrusion.

As per claim 2, the references as combined above disclose the claimed method of claim 1. **Erikson** further discloses configuring the FPGA using configuration data, for example (see column 3, lines 39-42). Therefore, this claim is rejected on the same rationale s the rejection of claim 1 above.

As per claim 3, the references as combined above disclose the claimed method of claim 2. **Erikson** further discloses the limitation of further comprising: transmitting the fingerprint from the FPGA to an encryption circuit, for example (see column 3, lines 31-32); encrypting the configuration data using the fingerprint as an encryption key, for example (see column 3, lines 30-35); and storing the encrypted configuration data in the storage device, for example (see column 3, lines 15-18).). Therefore, this claim is rejected on the same rationale s the rejection of claim 1 above.

As per claim 4, the references as combined above disclose the claimed method of claim 1. **Erikson** further discloses the limitation of wherein the fingerprint generated during power-up of the FPGA, for example (see column 3, lines 25-30). Therefore, this claim is rejected on the same rationale s the rejection of claim 1 above.

As per claim 12, Nassif substantially discloses a fingerprint element for generating fingerprint comprising: *first and second oscillators and sensing circuit including means for counting a first number of oscillations of a first oscillator and means for counting a second number of oscillations of a second oscillator during a predetermined time interval* (see column 4, lines 56-67) and the number of oscillations is counted over a fixed time interval (see column 4, lines 2-8)*;* **Nassif** discloses *means for generating a ratio between the first number and the second number of oscillations that represents an inherent manufacturing characteristic unique* (see column 4, lines 56-67). **Nassif** does not explicitly disclose the circuit is programmable (i.e. an FPGA). Use of programmable integrated circuit is notoriously well-known in the art of

cryptography. **Erickson** in an analogous art teaches a programmable integrated circuit as an FPGA and method for securing data used to configure a PLD or FPGA (see column 1, lines 5-15 and line 59 through column 2, line 49); a plurality of configurable logic elements within the FPGA being programmable with configuration data to implement a desired circuit design, for example (see column 3, lines 5-21);. **Erickson** further discloses key generator for generating a key that meets the recitation of *fingerprint element for generating fingerprint that represents an inherent manufacturing characteristic unique to the FPGA and transmitting encrypted configuration data from the storage device to the FPGA*, for example (see column 3, lines 34-36); *and a decryption circuit coupled to received encrypted configuration data, the decryption circuit configured to decrypt the encrypted configuration data in the FPGA using the fingerprint as a decryption key to extract the configuration data*, for example (see column 3, lines 34-42). See also column 2, lines 23-37. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of characterizing the circuit disclosed by **Nassif** into a programmable circuit so as to determine the performance of the circuit and to determine whether or not they exceed a certain design criteria as suggested by **Nassif** (see column 1, lines 15-30) and one of ordinary skill in the art would have recognized the benefits of using as FPGA as taught by **Erickson** for protecting the circuit designs from illegal copying and use (see column 1, lines 26-39).

Nassif discloses generating a ratio from dividing the number of two oscillations from two oscillators and further discloses that the ratio of the oscillation periods is proportional to the ratio of the capacitance but does not explicitly disclose using the ratio of the oscillators or capacitance as a key or fingerprint for cryptographic operation such as decryption of encrypted data.

Kawano et al in an analogous art teaches using the ratio of the capacitance for forming a specific code for the purpose of encryption/decryption (see column 19, lines 30-50 and column 26, lines 30-41). Therefore, since the ratio of the oscillation periods is proportional to the ratio of the capacitance, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the features as taught by **Kawano et al** of using the ratio of the capacitance as a fingerprint or key for the purpose of protecting secret data against intrusion (see column 1, lines 5-12) to modify **Nassif** and use the ratio of the oscillations as a fingerprint or key. As disclosed in **Kawano et al** the motivation for the combination would be to protect secret data against intrusion.

As per claim 13, the references as combined above disclose the claimed FPGA of claim 12. **Erikson** further discloses a configuration circuit for configuring the FPGA using configuration data, for example (see column 3, lines 39-42). Therefore, this claim is rejected on the same rationale s the rejection of claim 12 above

As per claim 15, the references as combined above disclose the claimed FPGA of claim 12. **Erikson** further discloses transmitting the fingerprint from the FPGA to an encryption circuit, for example (see column 3, lines 31-32); encrypting the configuration data using the fingerprint as an encryption key, for example (see column 3, lines 30-35); and storing the encrypted configuration data in the storage device, for example (see column 3, lines 15-18). Therefore, this claim is rejected on the same rationale s the rejection of claim 12 above

As per claim 44, the references as combined above disclose the claimed method of claim 1 wherein the generating the ratio is obtained by dividing the first number of oscillations by the second number of oscillations (see **Nassif**, column 3, lines 36-37).

4. **Claims 7 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,963,043 to **Nassif** in view of US Patent 5,970,142 to **Erickson** in view of US Patent 6,233,339 to **Kawano et al** as applied to claims 1 and 12 and further in view of US Patent 6,005,829 to **Conn**.

As per claims 7 and 21, Nassif does not explicitly disclose the oscillators comprise configurable logic blocks. **Conn** in an analogous art teaches oscillator circuit comprises configurable logic blocks as a well-known circuit (see column 3, lines 8-20 and column 5, lines 34-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the oscillators comprising configurable logic blocks as a design choice for the predictable result of making it adaptive to configuration control as well-known feature.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO form 892.

5.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carl Colin whose telephone number is 571-272-3862. The examiner can normally be reached on Monday through Thursday, 8:00-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser G. Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.C./

Carl Colin
Patent Examiner
August 18, 2007

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8/20/07